IN THE CLAIMS

Please cancel claims 7-11, 16-17, 21, and 29.

Please amend claims 1, 8, 18-19, and 27 as follows below.

The following listing of claims replaces all prior listing of claims.

1 1. (Currently Amended)   A microprocessor including:

2   a memory controller to couple to a memory and one or

3 more microprocessors;

4   an execution unit coupled to the memory controller,

5 the execution unit to trigger a snoop if a store into [[a]]

6 the memory occurs;

7   a trace cache coupled to the execution unit;

8   an instruction decoder coupled to the trace cache; and

9   [[a]] an instruction translation lookaside buffer

10 [[(TLB)]] (ITLB) having a content addressable memory (CAM),

11 the ITLB to receive and receiving a physical address

12 indicating the location where the store occurred in the

13 memory, the [[TLB]] ITLB to store page translations between

14 a linear page address and a physical page address pointing

15 to a page of the memory having contents stored within [[a]]

16 the trace cache, the [[TLB]] ITLB including a first CAM

17 input port responsive to the snoop to compare the physical

18 address received by the [[TLB]] ITLB with the physical page

19 address stored therein.

1   2. (Unamended)   The microprocessor of claim 1 wherein

2   if it is determined that the physical address received

3   by the TLB matches a physical page address stored within

4   the TLB, indicating that information was modified within

5   the memory correlating to information potentially located

6   within the cache, information within the cache is

7   invalidated.

1   3. (Unamended)   The microprocessor of claim 2 wherein

2   information within the cache is invalidated by setting

3   a bit in the cache to indicate invalid information in a

4   cache line and disregarding the information within the

5   cache.

1   4. (Unamended)   The microprocessor of claim 1 wherein

2   if it is determined that the physical address received

3   by the TLB matches a physical page address stored within

4   the TLB, indicating that information was modified within

5   the memory correlating to information potentially located

6   within the cache or a pipeline, and the microprocessor

7   provides inclusion for the cache and the pipeline such that

8   information within the cache and the pipeline are

9   invalidated.

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1   5. (Unamended)   The microprocessor of claim 4 wherein

2   information within the cache and a pipeline are

3   invalidated by setting a bit in the cache to indicate

4   invalid information in a cache line and disregarding the

5   information within the cache and the pipeline.

1   6. (Unamended)   The microprocessor of claim 4 wherein

2   the TLB maintains original page translations for all

3   bytes of information within the cache and pipeline to

4   provide inclusion.

1   7-11. (Canceled)

1   12. (Unamended)   The microprocessor of claim 1 wherein

2   the cache is a trace instruction cache and the

3   information stored therein is instructions and the TLB is

4   an instruction translation lookaside buffer (ITLB).

1   13. (Unamended)   A method of self modifying code detection

2   for cache coherency, comprising:

3   storing page table translations, the stored page table

4   translations including linear page addresses associated

5 with physical page addresses into a physically addressable

6 memory for information stored into a cache memory;

7 providing a physical memory address of a store into

8 the physically addressable memory; and

9 comparing the provided physical memory address to the

10 physical page memory addresses included in the stored page

11 table translations to determine if the physically

12 addressable memory has been updated by self modifying code.

1 14. (Unamended) The method of claim 13 wherein

2 the comparing generates a match between the provided

3 physical memory address and one or more of the physical

4 page memory addresses included in the stored page table

5 translations indicating the potential occurrence of self

6 modifying code and cache incoherency.

1 15. (Unamended) The method of claim 14 further comprising:

2 invalidating the instructions within the cache memory

3 and an instruction pipeline for execution and fetching new

4 instructions from the physically addressable memory to

5 overwrite the invalidated instructions after the comparing

6 generates a match indicating the potential occurrence of

7 self modifying code and cache incoherency.

1   16-17. (Cancelled)

1   18. (Currently Amended)   The method of claim 13 further

2   comprising:

3   maintaining original stored page table translations

4   for all bytes of information within the cache memory and an

5   instruction pipeline. [[.]]

1   19. (Currently Amended)   A computer including:

2   a memory; and

3   at least one microprocessor, the at least one

4   microprocessor including,

5   an instruction cache to store instructions

6   for execution,

7   an execution unit coupled to the instruction

8   cache to execute the instructions stored therein,

9   the execution unit to trigger a snoop if a store

10   into the memory is executed, and

11   an instruction translation lookaside buffer

12   (ITLB) having a content addressable memory (CAM),

13   the ITLB to receive ~~and receiving~~ a physical

14   address indicating the location where the

15   execution of the store occurred in the memory,

16   the ITLB to store page translations between a

17   linear page address and a physical page address

18   pointing to a page of the memory having contents

19   stored within the instruction cache, the ITLB

20   including a CAM input port responsive to the

21   snoop to compare the physical address received by

22   the TLB with the physical page address stored

23   therein.

1   20. (Unamended)   The computer of claim 19 wherein

2   if it is determined that the physical address received

3   by the TLB matches a physical page address stored within

4   the ITLB, indicating that an instruction was modified

5   within the memory correlating to an instruction located

6   within the instruction cache, instructions within the

7   instruction cache and an instruction pipeline within the

8   execution unit are invalidated.

1   21. (Cancelled)

1   22. (Unamended)   The computer of claim 19 wherein

2   the instruction cache is a trace instruction cache.

1   23. (Unamended)   A method of detecting cache incoherency in

2   a computer comprising:

3   providing a physical address associated with a store

4   into memory;

5   comparing the physical address associated with the

6   store into memory with a plurality of physical page

7   addresses indicating from what pages in a memory

8   information was stored into a cache;

9   generating a self modifying code hit signal indicating

10   a possibility of cache incoherency; and

11   invalidating the information stored into the cache

12   upon generation of the self modifying code hit signal.

1   24. (Unamended)   The method of claim 23 wherein

2   the plurality of physical page addresses are stored

3   within an instruction translation lookaside buffer.

1   25. (Unamended)   The method of claim 23 further comprising:

2   invalidating the information stored into an

3   instruction pipeline from the cache upon generation of the

4   self modifying code hit signal.

1   26. (Unamended)   The method of claim 23 further comprising:

2   fetching instructions from memory to rewrite the

3   information into the cache to obtain cache coherency.

1   27. (Currently Amended)   A microprocessor including:

2   a memory controller to couple to a memory and one or

3   more microprocessors, the memory controller to trigger a

4   snoop if a store into a memory occurs;

5   an execution unit coupled to the memory controller,

6   the execution unit to execute instructions; and

7   a translation lookaside buffer (TLB) coupled to the

8   execution unit, the TLB having a content addressable memory

9   (CAM), the TLB to receive and receiving a physical address

10   indicating the location where the store occurred in the

11   memory, the TLB to store page translations between a linear

12   page address and a physical page address pointing to a page

13   of the memory having contents stored within a cache, the

14   TLB including a CAM input port responsive to the snoop to

15   compare the physical address received by the TLB with the

16   physical page address stored therein.

1   28. (Unamended)   The microprocessor of claim 27 wherein

2   if it is determined that the physical address received

3   by the TLB matches a physical page address stored within

4   the TLB, indicating that information was modified within

5   the memory correlating to information potentially located

6   within the cache or a pipeline, and the microprocessor

7   provides inclusion for the cache and the pipeline such that

8   information within the cache and the pipeline are

9   invalidated.

1   29. (Cancelled)

1   30. (Unamended)   The microprocessor of claim 27 wherein

2   the cache is a trace instruction cache and the

3   information stored therein is instructions and the TLB is

4   an instruction translation lookaside buffer (ITLB).